CLAIMS

What is claimed is:

1. A method of preparing data for transmission, the method comprising:

transmitting a first signal requesting to transmit data;

generating a first portion of a first packet from data of a first source prior to receiving a second signal granting the permission to transmit data;

transmitting a third signal requesting a change of data source from the first source to a second source subsequent to said generating of said first portion; and

generating a second data packet from data of the second source.

2. The method of Claim 1, wherein said transmitting the third signal occurs if the data of the first source is incomplete.

3. The method of Claim 1, wherein said transmitting the third signal occurs if a time stamp included in the data of the first source is later than the time of receiving the second signal.

4. The method of Claim 1, further comprising:

discarding the first portion of the first data packet.

5. The method of Claim 1, wherein said transmitting of the third signal occurs after said receiving of said second signal.

6. A circuit comprising:

a refetch logic comprising:

a first data port;

a second data port;

a data bus;

a first control line;

a first terminal;

wherein the refetch logic propagates the data from the first data port to the data bus by default, the refetch logic propagating the data from the second data port to the data bus when a first control signal is active on the first terminal.

a link controller comprising:

a third data port coupled to the data bus;

a second terminal coupled to the first control line;

wherein the link controller reads data from the third data port and generates a first data packet, the link controller discarding the first data packet when a second control signal is active on the first control line.

7. The circuit of Claim 6, wherein the link controller generates a second packet when the second control signal is active.

8. The circuit of Claim 6, wherein the refetch logic further comprises:

a state machine comprising;

a second control line carrying a third control signal;

a multiplexer comprising:

a first multiplexer port coupled to the first data port;

a second multiplexer port coupled to the second data port;

a third terminal coupled to the third control line;

a third multiplexer port coupled to the third data bus;

wherein the multiplexer propagates the data from the first multiplexer port to the third multiplexer port by default, the

multiplexer propagating the data from the second data port to the third multiplexer port when the third control signal is active.

9. The circuit of Claim 6, wherein the link controller comprises:

a second state machine comprising:

a fourth control line carrying a fourth control signal;

a packet transmitter comprising:

a fourth data port coupled to the third data bus;

a fourth terminal coupled to the fourth control line;

wherein the packet transmitter reads data from the fourth data port and generates a first data packet, the packet transmitter discarding the first data packet when the fourth control signal is active.

10. The circuit of Claim 9, wherein the packet transmitter generates a second packet when the fourth control signal is active.

11. The circuit of Claim 6, further comprising an application logic having:

a first data bus coupled to the first data port;

a second data bus coupled to the second data port;

a fifth control line carrying a first control signal coupled to the first terminal.

added A1

add B4